

WHAT IS CLAIMED IS:

- 1 1. A package for a semiconductor device comprising:
2 a semiconductor die having a laterally conducting structure and a ground
3 contact on an upper surface; and
4 a leadframe comprising,
5 a diepad in contact with a lower surface of the die,
6 a lead separated from the diepad, and
7 a supplemental downbond diepad portion projecting from a main
8 portion of the diepad and configured to receive a downbond wire from the
9 ground contact.
- 1 2. The package of claim 1 wherein the supplemental diepad portion is
2 positioned on an end of the package between the lead and a second lead that is also separate
3 from the diepad.
- 1 3. The package of claim 1 further comprising a second lead projecting
2 from the diepad.
- 1 4. The package of claim 3 wherein the supplemental diepad portion
2 comprises a part of the second lead.
- 1 5. The package of claim 1 comprising more than one supplemental
2 downbond portion.
- 1 6. The package of claim 1 wherein the die comprises a power IC die.
- 1 7. The package of claim 1 wherein the die is configured to operate with a
2 current of between about 1 and 20 Amps.
- 1 8. The package of claim 1 wherein the die is selected from the group
2 consisting of an integrated circuit, a JFET, and a lateral MOSFET.
- 1 9. The package of claim 1 wherein the diepad comprises copper.
- 1 10. A method of packaging a laterally conducting semiconductor die, the
2 method comprising providing a supplemental diepad portion to receive a downbond wire

3 from a ground contact on an upper surface of the die, such that area of a main portion of the
4 diepad need not be allocated to receive the downbond wire and can instead be occupied by
5 the laterally conducting die.

1 11. The method of claim 10 wherein the supplemental diepad portion is
2 provided on an end of the package between two leads separate from the diepad.

1 12. The method of claim 10 wherein the supplemental diepad portion is
2 provided on a side of the package as a part of a lead projecting from the diepad.

1 13. The method of claim 10 wherein the leadframe supports a power IC
2 die.

1 14. The method of claim 10 further comprising providing more than one
2 supplemental diepad portion.

1 15. The method of claim 10 wherein the leadframe supports a die operated
2 with a current of between about 1 to 20 Amps.

1 16. The method of claim 10 wherein the leadframe supports a die selected
2 from the group consisting of an IC, a lateral MOSFET, and a JFET.